

High Electron Mobility in Strained Nanowires

Joey Gaffney

Department of Engineering Physics, University of British Columbia, Vancouver, BC V6T 1Z4, Canada

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Semiconductor nanowires are a prime candidate for gate-all-around field-effect transistors (FETs) due to their inherent morphology. As such, this has become a highly researched area in nanostructure devices. However, the electrical properties of nanowires are hampered by the increased surface-to-volume ratio leading to a higher density of edge effects. Electron mobility was consistently found to be lower than that of the bulk semiconductor material. That is, until recently, when a method of inducing a strain on nanowires by using a core/shell structure with a lattice spacing mismatch was shown to improve electron mobility. Here, the strain is measured using micro-Raman scattering spectroscopy and the electron mobility is measured using optical-pump Terahertz-probe spectroscopy (OPTPS). An overall improvement in electron mobility of 30% for strained nanowires over the bulk material was found, thus opening up the opportunity for major advancements in high-performance devices with integrated nanowires.

I. INTRODUCTION

Transistors are the basis for the technology of today. Since their invention, significant work has been done to reduce their size and improve their performance characteristics. Indeed, the transistor industry has advanced incredibly with modern devices, such as cell phones, now containing billions of transistors. As their size decreases, major advancements in transistors becomes more of a necessity. Fundamental design changes, material advancements, and new fabrication methods have had to be created in order to continue scaling down these devices. One such innovation is semiconductor nanowires.

Nanowires have become one of the most active research areas in the nanoscience community within the last 30 years [1]. These are a new class of semiconductors with a wire morphology and typical cross-sectional dimensions ranging from 1 to 100 nanometers. They are inherently suitable for use in gate-all-around field-effect transistors which allow for best control of the channel potential. Two basic approaches for the synthesis of nanowires are top-down, where a large piece of material is reduced to a smaller size through a process such as milling, and bottom-up, where the nanowire is grown by combining constituent atoms [2, 3]. This technology has opened up a wide variety of research for uses in transistors [4] as well as thermoelectronics [5] and optoelectronics [6].

However, semiconductor nanostructure research is disjointed from much of the research in traditional bulk semiconductors which make up the majority of transistors today. This means that most of the research around nanowires looks to make discoveries with sparse comparisons being made to the bulk material. Yet, as research has progressed from theory into experiment, these comparisons are necessary in order to realize promising new technologies and bring them into industry. One of the most important properties of semiconductors

is electron mobility. This is proportional to the drift current that can flow through the material and, as such, having a high electron mobility is great for applications in high-speed and low-power devices. Therefore, investigating the electron mobility of nanowires is of great interest in answering the question of whether nanowires could be implemented as the newest class of transistors. As such, the main paper that will be discussed here is "high electron mobility in strained GaAs nanowires," Balaghi et al (2021) [7].

II. PREVIOUS STATE OF THE ART

On an investigation of the electron mobility of various nanowire compositions (GaAs, InAs, and InP) it was found that the performance in general was worse than the bulk material [8]. This can be due to scattering from the wire boundaries or edge effects, where the atoms at the surface of the nanowires are not fully bonded to the neighboring atoms and act as a source of defects [9]. Thus, it is expected that smaller diameter nanowires would have a higher density of surface defects and exhibit lower mobility values. However, previous research has calculated that the electron mobility can be improved by introducing a tensile strain along the axis of the nanowire [10]. Not only does this reduce the edge effects, but it also allows for a reduction of the material band gap. This also predicts that the effective mass of electrons in the conduction band would decrease leading to improved mobility.

The best methods for controlling this strain were found to be growing core/shell nanowires with a lattice spacing mismatch [11]. This process involves growth of a core GaAs nanowire followed by growth of a much wider shell around it with a composition that has an adjustable lattice spacing based on the doping content. For instance, having a GaAs/ $\text{In}_x\text{Al}_{1-x}\text{As}$ core/shell structure would have a core lattice spacing of 5.65Å and a shell lattice spacing which depends on x as per

Vegard's Law as shown in equation (1).

$$\begin{aligned} a(x) &= a(XZ) \cdot x + a(YZ) \cdot (1 - x), \\ a(x) &= 6.0584x + 5.66 \cdot (1 - x). \end{aligned} \quad (1)$$

Additionally, the core/shell structure helps to mitigate some of the edge effects that are on the core itself by providing structural support around the perimeter. The tradeoff is an increase in overall diameter, although still within the nanometer range.

With a method of applying an axial tensile strain on the nanowires and the theory suggesting an improvement in the overall electron mobility, all that was left was to conduct an investigation into whether the use of strained nanowires improved electron mobility over the bulk material. This, as mentioned previously, would be a big step into bringing this new technology closer to manufacturing in industry.

III. RESULTS AND DISCUSSION

In the paper by Balaghi et al. [7] the main material investigated is the GaAs/In_{0.37}Al_{0.63}As core/shell nanowire. In particular, it looks at free-standing nanowires which are grown on Si(111) substrates by solid-source molecular beam epitaxy, a bottom-up method. As discussed, this lattice spacing mismatch leads to an overall tensile strain on the core of the nanowire. The core itself is around 22 nanometers thick while the shell is around 80 nanometers. This makes it so that even though the strain is also on the shell, because the volume of the shell is much larger than the core, the strain on the shell is negligible.

One thing to note is that Balaghi et al. investigates two types of core/shell nanowires: capped and uncapped. The only difference being that the capped nanowires are overgrown with a 5-nm-thick lattice-matched In_yGa_{1-y}As capping shell in order to protect the Al-containing shell from oxidation in air. The results between capped and uncapped nanowires are found to be very similar so I will be referring mainly to the uncapped nanowire results moving forward.

This strain on the GaAs core is measured using micro-Raman scattering spectroscopy. This involves shining a laser light on the material which interacts with the phonons in the material. This interaction results in the energy of the laser photons being shifted up or down. A strain on the core is expected to shift the energy of the Raman scattering for core phonons. Results of this measurement are shown in figure 1. The dashed vertical line indicates the peak position of bulk GaAs. A downshift of the GaAs peak in the obtained data is observed. This is attributed to a tensile strain on the core. The transverse optical (TO) and longitudinal

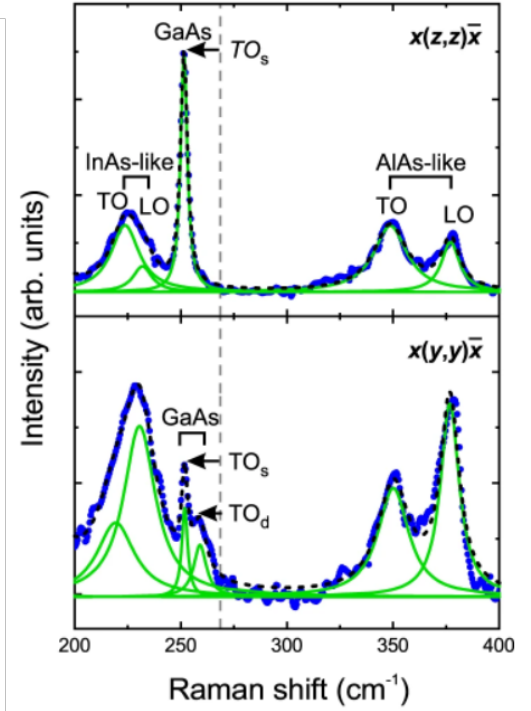


FIG. 1. Raman scattering spectra at room temperature from a single nanowire in two different polarisation configurations: $x(z,z)\bar{x}$ at the top and $x(y,y)\bar{x}$ on the bottom. The measured data is in blue and fitted curves in green. This figure is reproduced from Ref. [7]

optical (LO) phonons from the shell are seen in the ranges of 220-230 cm⁻¹ and 350-375 cm⁻¹ for InAs and AlAs respectively. These are in agreement with the corresponding bulk material thus indicating a largely unstrained shell.

The strain can be deduced using a hydrostatic deformation analysis but it is also measurable in other ways. In particular it is expected that the bandgap should be reduced. The bandgap for strained nanowires is measured using photoluminescence (PL) spectroscopy to be 1.1eV at room temperature compared to the 1.453eV of unstrained nanowires. This agrees with the simulations which are shown in figure 2. This energy dispersion then directly predicts the electron effective mass with the results being a reduction from 0.067 m_0 in the unstrained nanowire core to 0.0514 m_0 in the strained nanowire core.

Once this strain is confirmed, the next thing to measure is the corresponding electron mobility. This is performed using optical-pump Terahertz-probe spectroscopy (OPTPS). This technique involves sending an optical pulse to excite the sample followed after a short delay by a probing Terahertz signal. The transmitted pulses are measured to give the photoconductivity of the sample. The optical pulse is chosen with a specific photon energy, wavelength, and duration to generate

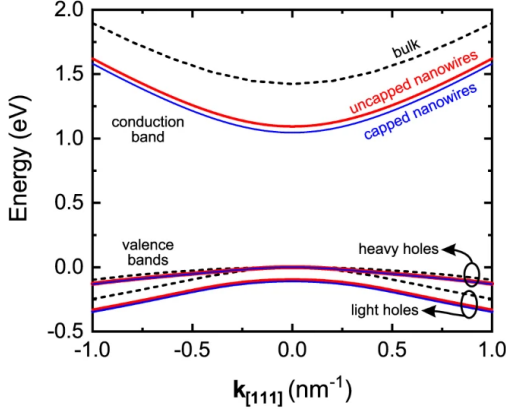


FIG. 2. Simulated energy dispersion for strained nanowires (red and blue curves) and bulk GaAs (black dashed curve) along the [111] crystallographic orientation. Two valence bands are shown, one for heavy holes and the other for light holes. This figure is reproduced from Ref. [7]

electrons and holes only inside only the core. Then, the THz signal drives plasmon oscillations of the generated charge carriers. Through varying the delay time, τ , a time-domain spectroscopy is obtained which allows for measurement of the complex conductivity spectrum, $\Delta\sigma(\omega, \tau)$. This can be fitted using a Lorentzian of the form in equation (2) along with the average carrier density in equation (3).

$$\Delta\sigma(\omega) = \frac{ine^2\omega}{m_e^*(\omega^2 - \omega_0^2 + i\omega\gamma)} \quad (2)$$

$$n = \frac{m_e^*\epsilon_r\epsilon_0}{ge^2}\omega_0^2 \quad (3)$$

$$\mu_e = \frac{e}{m_e^*\gamma} \quad (4)$$

Here, ω is the driving frequency, ω_0 is the surface plasmon resonance frequency given by $\text{Max}(Re\Delta\sigma)$, γ is the electron momentum scattering rate, m_e^* is the effective electron mass, e is the electron charge, g is the geometrical factor, $\epsilon_r = 14.16$ is the electric permittivity of the strained nanowire and ϵ_0 is the permittivity of free space.

Once γ is obtained from the fit, the electron mobility can be calculated using equation (4). One thing to note is that this model assumes that the peak width of $Re\Delta\sigma$ is dictated only by γ but it can be broadened when the density of nanowires is increased (thus resulting in an increased signal-to-noise ratio) as inevitably there will be nanowires in close proximity or even in contact with one another which influences the results. From the results, it was found that a dense area (filling factor

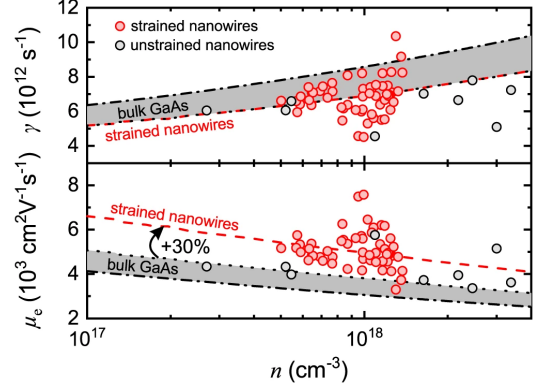


FIG. 3. Electron momentum scattering rate (top) and electron mobility (bottom) for strained nanowires, unstrained nanowires, and bulk GaAs. All of the data comes from OPTPS measurements at room temperature. The two reference curves for bulk GaAs come from [12] and [13] This figure is reproduced from Ref. [7]

FF= 0.28%) had a 70% larger peak width than a sparse area (FF= 0.28%) resulting in a 41% lower mobility. Thus, the results from OPTPS can be regarded as a lower limit for the real value of a single isolated nanowire.

The overall results for the mobility in strained nanowires is shown in figure 3. A remarkable result is that the strained nanowires exhibit higher mobility than both unstrained nanowires and the bulk GaAs as obtained from two past research studies [12], [13]. The relative increase in mobility from bulk GaAs to the strained nanowires is around 30%. One thing to note is that the reported values for unstrained nanowires is the highest yet and this is attributed to both the high structural quality of the nanowires and the lower filling factor used on their samples.

These results are expected to be enhanced with further research. Inherent in the OPTPS method is scattering of electrons by photo-generated holes. If this effect is excluded, as it would be in the case of high-electron mobility transistors, then an increase of around 50% for mobility is predicted. Additionally, using an even larger lattice mismatch to induce more strain on the nanowire core is expected to improve electron mobility even further. However better growth methods are required as there are inherent structural problems during growth when the strain is large. For instance, if the growth rate is too slow or the growth is not homogeneous then the strain of the shell causes the nanowire to buckle [11].

Beyond this, the findings from this work are relevant for systems beyond GaAs and it provides a framework for strained/core shell nanowires in general. This has the potential to trigger major advancement in high-performance nanowire electronic devices. As such, future work such as finding ways to implement

this technology into CMOS is a critical step forward. Further enhancing the process flow for growth epitaxy to incorporate larger core strain is also a topic that needs further research.

IV. CONCLUSION

Nanowires are a very active area of research but only recently have comparisons been drawn to bulk semiconductor material. They benefit from a morphology which makes them suited for gate-all-around field-effect transistors but their characteristic electron mobility was lower than that of the bulk material on account of the large surface-to-volume ratio which meant a larger concentration of edge effects. Previous theories had predicted that applying an axial tensile strain to nanowires could increase some electrical properties such as electron mobility [10]. But it wasn't until recently that reliable methods for implementing this strain came about in the form of a core/shell nanowire structure with a lattice spacing mismatch [11]. Using micro-Raman scattering

spectroscopy to measure the strain and optical-pump Terahertz probe spectroscopy (OPTPS) to measure the mobility, it was found that the electron mobility in strained nanowires was not only higher than unstrained nanowires, but also 30% higher than the bulk material.

These results provide a roadmap for all strained nanowire devices toward the development of new high-speed low-power devices. Further research will be needed to reach this point, in both integration and growth methods. Measuring the speed and power consumption of CMOS devices which incorporate these strained nanowires would be crucial in evaluating their performance to be used in industry. However to reach that point, more research into the limits of this lattice-mismatch induced strain are necessary. With better growth methods, it is predicted that the tensile strain on the core can be increased further with a higher indium doping concentration of the shell. This in turn leads to a significant increase in the electron mobility. These small optimizations in growth and electrical properties are crucial for the major advancements that researchers hope to make with the use of nanowires.

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